IN THE CLAIMS

Please cancel claims 1-12 without prejudice.

Please add claims 13-33 as follows:

~~Patent Claims~~WHAT IS CLAIMED IS:

1-12. (Cancelled)

13. (New) A memory arrangement comprising:

a plurality of rewriteable memory cells arranged at crossovers between word lines and bit lines, wherein the memory cells are configured such a that the information stored in the memory cells is read out in a nondestructive manner; and

wherein the memory arrangement has a flag cell either for each word line or for each bit line, the flag cell being able to store an item of information that indicates whether at least one of the memory cells either along the respective word line or along the respective bit line has been subjected to a reading operation since a basic state occurred.

14. (New) The memory arrangement as claimed in claim 13, comprising wherein the flag cells are of the same memory cell type as the memory cells.

15. (New) The memory arrangement as claimed in claim 14, comprising wherein the flag cells are of a memory cell type in which the stored information can be read out in a nondestructive manner.

16. (New) The memory arrangement as claimed in claim 13, comprising wherein the flag cells are of a memory cell type in which the stored information can be read out in a nondestructive manner.

17. (New) The memory arrangement as claimed in claim 13, comprising wherein the flag cells are of the nonvolatile type.

18. (New) The memory arrangement as claimed in claim 13, comprising wherein the memory arrangement is an individual memory chip.

19. (New) The memory arrangement as claimed in claim 13, comprising wherein the memory arrangement is a plurality of memory chips that are assigned to one another.

20. (New) The memory arrangement as claimed in claim 13, comprising wherein the memory arrangement has a refresh device for carrying out a refresh operation.

21. (New) A method for operating a memory arrangement having rewritable memory cells which are arranged at crossovers between word lines and bit lines, in which arrangement the memory cells comprising:

reading out information stored in the memory cells in a nondestructive manner; and subjecting those memory cells which are arranged either along a word line or along a bit line along which at least one reading operation has previously taken place, to a refresh operation.

22. (New) The method as claimed in claim 21, comprising:

storing the occurrence of a reading operation as such as information in a flag cell that is arranged either along a word line that is affected by the reading operation or along a bit line that is affected by the reading operation.

23. (New) The method as claimed in claim 21, comprising:

resetting the information stored in the affected flag cells to a standard value when carrying out the refresh operation.

24. (New) The method as claimed in claims 21, comprising:

triggering the carrying-out of the refresh operation by another given event.

25. (New) A memory arrangement comprising:

rewritable memory cells which are arranged at crossovers between word lines and bit lines, in which arrangement the memory cells are configured in such a manner that the information stored in the memory cells is read out in a nondestructive manner;

a refresh device for carrying out a refresh operation;

a flag cell either for each word line or for each bit line, the flag cell being able to store an item of information that indicates whether at least one of the memory cells either along the respective word line or along the respective bit line has been subjected to a reading operation since a basic state occurred; and

wherein the refresh device is designed in such a manner that, for each flag cell, it carries out a refresh operation, in a manner dependent on the information stored in the flag cell, for those memory cells which are arranged along the word line or bit line associated with the flag cell.

26. (New) The memory arrangement as claimed in claim 25, comprising wherein the flag cells are of a memory cell type in which the stored information can be read out in a nondestructive manner.

27. (New) The memory arrangement as claimed in claim 26, comprising wherein the flag cells are of the nonvolatile type.

28. (New) The memory arrangement as claimed in claim 27, comprising wherein the memory arrangement is an individual memory chip.

29. (New) The memory arrangement as claimed in claim 28, comprising wherein the memory arrangement is a plurality of memory chips that are assigned to one another.

30. (New) The memory arrangement as claimed in claim 29, comprising wherein the memory arrangement has a refresh device for carrying out a refresh operation.

31. (New) The memory arrangement as claimed in claim 13, comprising wherein the flag cells are of the same memory cell type as the memory cells.

32. (New) The memory arrangement as claimed in claim 14, comprising wherein the flag cells are of a memory cell type in which the stored information can be read out in a nondestructive manner.

33. (New) A memory arrangement comprising:

a plurality of rewriteable memory cells arranged at crossovers between word lines and bit lines, wherein the memory cells are configured such a that the information stored in the memory cells is read out in a nondestructive manner; and

means for providing a flag cell either for each word line or for each bit line, the flag cell means being able to store an item of information that indicates whether at least one of the memory cells either along the respective word line or along the respective bit line has been subjected to a reading operation since a basic state occurred.